EFFICIENT TEST STRUCTURE FOR NON-VOLATILE MEMORY AND OTHER SEMICONDUCTOR INTEGRATED CIRCUITS

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ABSTRACT

A test system includes a test wafer having non-volatile memory dies and an exposed set of pads. A probe wafer includes test circuitry, a first set of pads exposed at a first surface, a second set of pads exposed at a second surface (opposite the first surface), and an interconnect structure. The interconnect structure includes traces that extend through the probe card or around the edges of the probe card, between the first and second surfaces. A prober aligns the test wafer with the probe wafer, such that the pads of the test wafer contact the first set of pads of the probe wafer. The prober further contacts the second set of pads of the probe wafer, and provides connections between these pads and a tester. The probe wafer is fabricated using semiconductor processing techniques, so that precise alignment exists between the test wafer and the probe wafer.